REMARKS

I. Introduction

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-2, 5 and 18 Under 35 U.S.C. § 103

Claims 1-2, 5 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 6,574,213. Applicant respectfully traverses this rejection for at least the following reasons.

In issuing the pending Office Action, other than cutting and pasting the argument raised with respect to claim 18 onto the rejection of claim 1, the Examiner's grounds of rejection are the same as previously set forth in the final Office Action dated January 25, 2005 (see, page 5 of final Office Action). Indeed, the Examiner's position with respect to the distinctive features of claims 1, 6 and 10 has not changed and is independent of the last amendment, which merely incorporates the claimed subject matter of claim 18 into each independent claim.

Furthermore, the Examiner has not responded to each and every detailed argument set forth in the amendment filed on March 24, 2005. For example, in the Office Action dated January 25, 2005, the Examiner acknowledged that "Anandakumar fails to disclose one or more MACs integrated onto a same chip as a processor," but suggested that it would have been obvious to one of ordinary skill in the art to modify the DSP processor 1511 of Anandakumar such that the MCU controller 1781 and the DSP processor 1511 are integrated onto a same chip because "Anandakumar discloses various parts of functions of the DSP and Microcontroller can be partitioned and stored-on chip as desired (see, page 4, lines 10-15 of Office Action dated January 25, 2005)."

In response, Applicant asserted, "[I]n the cited portion, Anandakumar discloses that adaptive rate/diversity operations (discussed in connection with FIG. 16) can be partitioned between various processors and the microcontroller of Anandakumar, and the adaptive rate/diversity operations can be stored in on chip or off chip memories" and "... does not suggest

in the cited portion that functions associated with the processor and the microcontroller (apart from the adaptive rate/diversity operations) can be partitioned and stored onto a same chip."

However, it does not appear that the Examiner has addressed the foregoing distinction(s) provided by the Applicant. The Examiner has neither explained nor provided factual evidence as to why the pending claims remain defective.

Accordingly, without a new rejection, response and reasoning in support of the Examiner's maintained rejection, it is difficult for the Applicant to provide a proper rebuttal. Accordingly, it is respectfully submitted that the deficiencies of the pending rejections as previously argued in the amendment filed March 24, 2005 are still a valid basis for the patentability of claim 1.

As a final note, if the pending rejection is maintained, it is respectfully requested that the foregoing arguments be addressed in the next Office Action so as to afford the Applicant an opportunity to respond to the concerns raised therein.

A. **Anandakumar Fails To Disclose An IEEE 802.3 Media Access Controller Integrated Onto A Same Chip As A Voice-over-IP Processor Core, and Coupled To a Voice-over-Internet Protocol Processor Core**

Claim 1 recites in-part "one or more IEEE 802.3 media access controllers (MACs) coupled to the Voice-over-Internet Protocol processor core through the bus."

As acknowledged by the Examiner in the pending rejection, Anandakumar fails to disclose one or more MACs integrated onto a same chip as a processor. The Examiner suggests that it would have been obvious to one of ordinary skill in the art to modify the DSP processor 1511 of Anandakumar such that the MCU controller 1781 and the DSP processor 1511 are integrated onto a same chip because "Anandakumar discloses various parts of functions of the DSP and Microcontroller can be partitioned and stored on-chip as desired (see col. 39, lines 1-10)." Applicant respectfully disagrees.

Specifically, it is respectfully submitted that the disclosure of Anandakumar has been taken out completely out of context. Indeed, Anandakumar discloses "various parts of the [DSP] improvements ... are suitably partitioned between the DSPs ... and stored on-chip and in the off-chip memories as desired." Accordingly, if anything, Anandakumar actually supports the patentability of the pending claims, because Anandakumar discloses only that the partitioning be stored in on-chip ***memories*** (i.e., separate memories) and is silent with respect to integrating the alleged repeater (echo canceller/gain control), the alleged communication port (PCM interface) and the MAC of the TCP/UDP/IP stack 1811 are on the ***same chip memory***.

Further, in the cited portion, Anandakumar discloses that adaptive rate/diversity operations (discussed in connection with Fig. 16) can be partitioned between various processors and the microcontroller of Anandakumar, and the adaptive rate/diversity operations can be stored in on-chip or off-chip memories.

Anandakumar, however, does ***not*** suggest in the cited portion that ***functions associated with the processor and the microcontroller*** (apart from the adaptive rate/diversity operations) ***can be partitioned and stored onto a same chip***.

In this regard, even assuming *arguendo* that the Examiner's position has merit, Applicant respectfully submits that claim 1 does not merely recite one or more IEEE 802.3 media access controllers (MACs), but also recites one or more IEEE 802.3 MACs ***coupled to the Voice-over-Internet Protocol processor core through the same bus***.

At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known (e.g., a media access controller, a Voice-over-Internet Protocol processor, a memory and communication ports) without providing a prima facie showing of obviousness that the ***combination*** or the ***inter-relationship*** (emphasis added) of these elements recited in the claims is known or suggested in the art.

That is, the proposed combination fails to arrive at the claimed invention, because the Examiner has not provided factual evidence to show the ***inter-relationship*** between the alleged MACs and the alleged Voice-over-Internet Protocol processor, and that the alleged MACs are coupled to the alleged Voice-over-Internet Protocol processor using the same bus as that coupled to the alleged repeater and alleged communication ports.

Absent this teaching, it is respectfully submitted that Anandakumar does not disclose "a protocol parser unit configured to direct the received transmission control protocol packets from the media access controller to the central processing unit," as recited in claim 1.

B. **Anandakumar Fails To Disclose A Repeater Integrated Onto A Same Chip As A Voice-over-IP Processor Core**

As is commonly known in the art, a repeater is a network device that repeats signals from one cable onto one or more other cables. Anandakumar discloses a DSP processor 1511 including a echo canceller block 1517 and a gain control block 1521. In the Office Action, the Examiner associates a repeater with the combination of the echo canceller block 1517 and gain control block 1521. Applicant respectfully disagrees.

While the echo canceller block 1517 may remove interference and the gain control block 1521 may strengthen signals (as acknowledged by the Examiner), the echo canceller block 1517 and the gain control block 1521 only does so ***in connection with signals received from the PCM interface 1515***. The echo canceller block 1517 and the gain control block 1521 does ***not*** repeat signals from one cable/bus onto one or more other cables/buses, as would a repeater. Accordingly, it is respectfully submitted that the echo canceller block 1517 and the gain control block 1521 cannot reasonably interpreted as functionally the same as that of a repeater.

If the pending rejection is maintained, Applicant respectfully requests that the Examiner provide technical publication and/or journals in support of such interpretation.

Anandakumar, therefore, fails to disclose a repeater integrated onto a same chip as a voice over processor core, as required by claim 1.

C. **The Claim Has Limitations Not Taught By Any Of The Cited References Above**

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970) (emphasis added). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability. . . . If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Anandakumar fails to disclose a processor that includes one or more IEEE 802.3 media access controllers (MACs) and a repeater that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core. The Examiner has not shown that Zimmerman or Edholm discloses a processor that includes one or more IEEE 802.3 media access controllers (MACs) and a repeater that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core. Consequently, neither Anandakumar, Zimmerman, nor Edholm (either alone or in combination) can render claim 1 obvious, and the Examiner has not made a *prima facie* showing of obviousness.

D. **No Motivation To Modify Anandakumar**

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. The teaching or suggestion to make the claimed combination must be found in the prior art. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Applicant respectfully submits that the Examiner has not provided any teachings from Anandakumar that support modifying Anandakumar such that the MCU controller 1781 and the DSP processor 1511 are integrated onto a same chip.

i. The Examiner Has Shown No Objective Teaching

In making a rejection under § 103, the Examiner can satisfy the burden of making a *prima facie* case of obviousness "only by showing some objective teaching." *In re Fritch*, 972 F.2d 1260, 1265 (Fed. Cir. 1992). As has often been noted, evidence of teaching or suggestion is "essential" to avoid the error of hindsight. *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988).

"The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citation omitted).

The Examiner's proposed motivation for modifying Anandakumar is that it would have been obvious to modify Anandakumar to integrate the MCU controller 1781 and the DSP processor 1511 onto a same chip in order to consolidate both VoIP processing and physical network interfacing functions in the same chip so that data and signaling communication overhead time between the MCU controller 1781 and the DSP processor 1511 will be shorter. This does not constitute a showing of some objective teaching – either in the references or in any other source. The invention of Anandakumar is ***not*** directed to reducing data and signaling communication overhead between the MCU controller 1781 and the DSP processor 1511.

Indeed, the alleged motivation does not appear to be found in Anandakumar. The Office Action appears to attempt to overcome the deficiencies of Anandakumar by asserting an opinion (i.e., no suggestion or support in the prior art) that one of ordinary skill in the art would have found it obvious to modify Anandakumar.

Thus, it is respectfully submitted that the alleged motivation is directed to an opinion rather than what is taught by the cited prior art. It is submitted that an opinion cannot be relied on to replace the deficiency of a prior art reference. If the pending rejection intended to take Official Notice that the differences between the cited prior art and the present invention as recited in the rejected claims are well-known in the art, then pursuant to **M.P.E.P. § 2144.03**, Applicant respectfully traverses such an assertion and requests the Examiner to cite one or more references in support of this allegation (see, second paragraph, last three lines of **M.P.E.P.**

§ 2144.03, which requires the Examiner to cite a reference in support of an allegation of Official Notice when Applicant traverses).

It is respectfully submitted that the proposed combination is based solely on improper hindsight reasoning, utilizing Applicant's specification inadvertently as a guide to pick and choose the selected elements from various references so as to reach the claimed invention.

Hindsight reconstruction, using applicant's claims as a template to reconstruct the invention by ***picking and choosing*** isolated disclosures from the prior art, is impermissible. For example, in *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), the Federal Circuit stated:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. (citations and quotations omitted)

Applicant respectfully submits that the Examiner has not provided any motivation to modify Anandakumar other than to rely on the level of skill in the art, which is impermissible. *See Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

Further, it has been judicially held that a ***generalization*** does not establish the requisite motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995). Rather, the PTO is required to point out wherein the prior art suggests modifying a reference or combining references to arrive at a specifically claimed invention. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1543 (Fed. Cir. 1998). In this respect, Applicant would, again, stress that ***the mere identification of claim features in disparate references does not establish the requisite realistic motivation*** to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).

For all of the foregoing reasons, the proposed combination fails to establish *prima facie* obviousness of the pending claims.

III. The Rejection Of Claims 4, 6, 8-10 and 12-15 Under 35 U.S.C. § 103

Claims 4, 6, 8-10 and 12-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Anandakumar in view of USP No. 6,526,131 to Zimmerman.

With respect to claims 6 and 10, the Examiner has rejected the foregoing claims based on the same reasons set forth in the rejection to claim 1. Accordingly, Applicant respectfully submits that the reasons discussed above with respect to claim 1 are also applicable to the rejection of claims 6 and 10, and claims dependent thereon.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is neither anticipated nor rendered obvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987).* Accordingly, as independent claims 1, 6 and 10 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

V. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

Applicant : Frank Preiss
Serial No. : 09/660,882
Filed : September 13, 2000
Page : 10 of 10

Attorney's Docket No.: 12754-120001 / 1999P07765US01

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: October 12, 2005

Alex Chan
Reg. No. 52,713

Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, California 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

50305865.doc